

IN THE CLAIMS:

1 1. (Original) A multiprocessor computer system having a plurality of processors  
2 interconnected so that they can share memory, comprising:  
3 a plurality of links, each link of said plurality of links connecting a processor to  
4 another processor;  
5 a router box (RBOX) associated with each processor of said plurality of proces-  
6 sors, said RBOX arranged to forward a message received on an input link of said plural-  
7 ity of links from a source processor to an outgoing link of said plurality of links toward a  
8 destination processor in response to data carried in said message;  
9 a plurality of microprocessors, each of said microprocessors having a microproc-  
10 essor memory associated therewith, a selected microprocessor of said plurality of micro-  
11 processors associated with at least one processor of said plurality of processors, said plu-  
12 rality of microprocessors arranged to control said plurality of processors, said control in-  
13 cluding applying electric power to a selected processor and removing electric power from  
14 said selected processor;  
15 a data structure stored in microprocessor memory, said data structure storing a  
16 representation of the links connecting said processors and storing routes used by said  
17 RBOX in routing messages along said links, a copy of said data structure stored in mi-  
18 croprocessor memory of each of said microprocessors; and,  
19 a process to update said data structure in each said microprocessor memory in the  
20 event that a change occurs in a status of a component of said multiprocessor computer  
21 system.

1 2. (Currently amended) The computer system apparatus of claim 1 further comprising:  
2 a process executing in said microprocessors for directing said microprocessors in  
3 formation of a partition of said processors, said partition having a selected number of said  
4 processors as members, said members capable of reading and writing a common memory

5 within said partition, and other non-member processors excluded from reading and writ-  
6 ing said common memory; and,

7 a second data structure for storing a representation of said partitions, and storing  
8 routes through said links for transfer of messages between processors within a partition  
9 but not between processors of different partitions.

1 3. (Currently amended) The computer system apparatus of claim 2 wherein the micro-  
2 processors are interconnected through a local area network, the system further compris-  
3 ing:

4 a management computer communicating through said local area network with  
5 said microprocessors, said management computer having an input device ~~such as a key-~~  
6 ~~board and mouse~~ for entering commands to said plurality of microprocessors to modify  
7 said second data structure ~~data-base~~ in order to establish the processors belonging to a  
8 partition, said multiprocessor computer system supporting a plurality of said partitions;  
9 and

10 a process responsive to said second data structure ~~data-base~~, said process execut-  
11 ing in said microprocessors to establish that a processor in a partition can read and write  
12 memory associated with other processors of said partition, but cannot read and write  
13 memory associated with processors which are not members of said partition.

1 4. (Currently amended) The computer system apparatus of claim 1 wherein the micro-  
2 processors are interconnected through a local area network, the system further compris-  
3 ing:

4 an input/output (IO) subsystem associated with at least one ~~selected~~ processors of  
5 said plurality of processors;

6 an IO microprocessor associated with each said IO subsystem, said IO microproc-  
7 essor communicating with said microprocessors through said local area network, each  
8 said IO microprocessor having an IO microprocessor memory holding a copy of said sec-  
9 ond data structure ~~-database~~;

10 a process executing in said IO microprocessor, said process responsive to said  
11 second data structure database, said process to apply power or remove power to said IO  
12 subsystem.

1 5. (Currently amended) The computer system apparatus of claim 1 further comprising:  
2 a boot-up process executing in microprocessors of said plurality of microproces-  
3 sors, said boot-up process to start execution of said processors of said multiprocessor  
4 system, and said multiprocessor system capable of continuing operation, after start of  
5 execution of said processors, to permit removal of a microprocessor from the multiproc-  
6 essor system without interrupting execution of said processors.

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1 6. (Original) A method for operating a multiprocessor computer system, comprising:  
2 connecting a plurality of processors so that they can share memory, a processor of  
3 said plurality of processors connected to another processor by at least one link of a plu-  
4 rality of links;  
5 associating a router box (RBOX) with each processor of said plurality of proces-  
6 sors, said RBOX arranged to forward a message received on an input link of said plural-  
7 ity of links from a source processor to an outgoing link of said plurality of links toward a  
8 destination processor in response to data carried in said message;  
9 interconnecting a plurality of microprocessors, each of said microprocessors hav-  
10 ing a microprocessor memory associated therewith, a selected microprocessor of said plu-  
11 rality of microprocessors associated with at least one processor of said plurality of proc-  
12 essors, said plurality of microprocessors arranged to control said plurality of processors,  
13 said control including applying electric power to a selected processor and removing elec-  
14 tric power from said selected processor;  
15 storing a data structure in microprocessor memory, said data structure storing a  
16 representation of the links connecting said processors and storing routes used by said  
17 RBOX in routing messages along said links, a copy of said data structure stored in mi-  
18 croprocessor memory of each of said microprocessors; and,

19 updating said data structure in each said microprocessor memory in the event that  
20 a change occurs in a status of a component of said multiprocessor computer system.

1 7. (Original) The method of claim 6, further comprising:

2 executing a process in said microprocessors for directing said microprocessors in  
3 formation of a partition of said processors, said partition having a selected number of said  
4 processors as members, said members capable of reading and writing a common memory  
5 within said partition, and other non-member processors excluded from reading and writ-  
6 ing said common memory; and,

7 storing in a second data structure a representation of said partitions, and storing  
8 routes in said second data structure through said links, said routes for transfer of mes-  
9 sages between processors within a partition but not between processors of different parti-  
10 tions.

1 8. (Currently amended) The method of claim 6, further comprising:

2 establishing communication between a management computer and said micro-  
3 processors through said local area network, said management computer having an input  
4 device ~~such as a keyboard and mouse~~ for entering commands to said plurality of micro-  
5 processors to modify said second data structure ~~data base~~ in order to establish the proces-  
6 sors belonging to a partition, said multiprocessor computer system supporting a plurality  
7 of said partitions;

8 establishing, in response to said second data structure ~~data base~~, that a processor  
9 in a partition can read and write memory associated with other processors of said parti-  
10 tion, but cannot read and write memory associated with processors which are not mem-  
11 bers of said partition.

1 9. (Currently amended) The method of claim 6, further comprising:

2 associating an input/output (IO) subsystem with selected processors of said plu-  
3 rality of processors;

4 associating an IO microprocessor with each said IO subsystem, said IO micro-  
5 processor communicating with said microprocessors through said local area network,  
6 each said IO microprocessor having an IO microprocessor memory holding a copy of  
7 said second data structure database;

8 executing a process in said IO microprocessor, said process responsive to said  
9 second data structure database, said process to apply power or remove power to said IO  
10 subsystem.

1 10. (Original) The method as in claim 6, further comprising:

2 executing a boot-up process in microprocessors of said plurality of microproces-  
3 sors, said boot-up process to start execution of said processors of said multiprocessor  
4 system, and said multiprocessor system capable of continuing operation, after start of  
5 execution of said processors, to permit removal of a microprocessor from the multiproc-  
6 essor system without interrupting execution of said processors.

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